CONFERENCE VENUE

The conference will be hosted in the upscale JW Marriott Bucharest Grand Hotel, conveniently situated downtown. Inaugurated in 2000, the hotel exudes an essence of European elegance and comfort, providing excellent facilities for any large-scale event. The convention center includes 12 reconfigurable rooms adding up to a total of 2044 m^2. The hotel is located next to the Parliament Palace, the largest building in Europe and the second largest in the world, right after the Pentagon.

The city of Bucharest is the capital of Romania and its most important cultural, business and financial center. A young and dynamic city, Bucharest has an eclectic architecture, which provides a view into its history. A mixture of medieval, neoclassical and Art Nouveau buildings, the city center also boasts recently built contemporary structures such as skyscrapers and office buildings. The city's majestic architecture and the sophistication of its elite earned Bucharest the nickname of "Little Paris" at the beginning of the 20th century.

Bucharest is easily accessible from all major European cities and with only one-stop connections from Asia and the Americas. The city benefits from a modern international airport and an extensive public transport system that is one of the largest in Europe.

Romania is the largest country in southeastern Europe and a member of the European Union since January 2007. The country is best known worldwide for its beautiful natural landscapes and UNESCO Heritage sites, such as The Danube Delta, the Monasteries of Moldova and the Transylvanian medieval cities. Also known as the mysterious land of the Legend of Dracula, Romania is a whole of fascinating experiences where Authentic, Natural and Cultural are the words that best capture its essence and make up an intriguing country rich in history, arts and scenic beauty.

CONTACT INFORMATION

Local Organization
BDR Associates, Hill + Knowlton Strategies Affiliate
1A Nikolai Gogol Street
Bucharest -1, 012017, Romania
essderc2013@bdr.ro

ORGANIZATION COMMITTEE

Conference Chairs
Michael Neuhäuser, Infineon Technologies Romania & CO SCS
Corneliu Burileanu, Politehnica Bucharest
Ion Bogdan, TU Iasi

ESSCIRC Chairs
Andrei Vladimirescu, Univ. of California at Berkeley & Institut Supérieur d'Electronique de Paris
Liviu Goras, TU Iasi

ESSDERC Chairs
Dan Dascalu, IMT Bucharest
Adrian Mihai Ionescu, Ecole Polytechnique Fédérale de Lausanne

SCHEDULE AT A GLANCE

Monday, 16 Sept 2013	Tutorials
Tuesday, 17 Sept 2013	Conference opening Technical sessions Welcome reception
Wednesday, 18 Sept 2013	Technical sessions Gala dinner
Thursday, 19 Sept 2013	Technical sessions Farewell
Friday, 20 Sept 2013	Workshops

KEYDATES

Submission deadline	15 April 2013
Notification of acceptance	7 June 2013

CONFERENCE WEBSITE

http://www.essderc.org

essderc 2013

Second Call for Papers

43rd Solid-State Device Research Conference (ESSDERC)

16-20 September 2013
Bucharest, Romania

Paper Submission Deadline
15 April 2013
Electronic submission

http://www.essderc.org

GENERAL PURPOSE OF THE CONFERENCE

The aim of ESSDERC conferences is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. ESSDERC and ESSCIRC (sister conference) are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts and circuits and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC will share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions. The main themes for original contributions to be submitted to ESSDERC 2013 include but are not limited to the following:

Advanced CMOS Devices

Ultimate CMOS scaling for high performance, low power and low voltage devices, novel MOS device architectures (double and multiple gate, vertical, ballistic), circuit/device interaction and co-optimization, high-mobility channel engineered devices, SOI, SGOI, and SiON devices; SiGe, Ge, and strained devices. 3D integrated circuits.

Process & Integration

Front-end and back-end processes for fabrication of logic memory and 3D integrated circuits, including: substrate technologies, gate dielectrics, high k, gate stack, junction technology, cleaning and surface preparation, litography, etching, isolation technologies, thin dielectrics, shallow junctions, silicides, 3D integration, interconnects, low k dielectrics, advances in integration for ULSI; SOI, SGOI; advanced/novel memory process integration; logic and mixed-mode IC manufacturing; RF integration (passives, active devices); photonics integration; multilevel interconnects, advanced packaging.

Microwave and power solid state devices

RF CMOS, analog and mixed signal devices, passives, antennas, filters, RF MEMS, Bipolar, BiCMOS, smart power devices, high-voltage, high power devices, high temperature operation, SiC devices, CMOS compatible power devices, IC cooling. Discrete and integrated high power/current/voltage devices. Integrated RF components including inductors, capacitors, and switches. Note: Microwave includes millimeter wave and shorter wavelength (frequencies up to the THz region).

Modelling and Simulation

Numerical, analytical and statistical modeling of solid-state electronic and optoelectronic devices, quantum mechanical and non-stationary transport phenomena, ballistic transport, compact circuit modeling for devices and interconnects, modeling and simulation of front-end and back-end fabrication processes, electro-thermal modeling and simulation.

Characterization, Reliability and Yield

Characterization techniques, parameter extraction, advanced test structures and methodologies, reliability issues for new materials and devices (reliability of high-k and low-k materials), reliability of advanced interconnects, ESD, soft errors, noise and mismatch behavior, bias temperature inestabilities, EMI, defect monitoring and control, metrology, impact of back-end processing on devices, manufacturing technologies for reliability, physics of failure analysis.

Advanced and Emerging Memories

Novel memory cell concepts, embedded and stand-alone memories, DRAM, FeRAM, MRAM, PCRAM, CBRAM, Flash, SONOS, nanocrystal memories, single and few electron memories, 3D IC stacks, organic memories, NEMS-based device, 3D integration, reliability and modeling.

MEMS, Bio-sensors and Display Technologies

Design, fabrication, modeling, reliability and packaging of all physical sensors and MEMS categories, bio-sensors for chemical, molecular and biological applications, BioMEMS, devices and technologies for lab-on-chip, integration of detectors, sensors, and actuators, CCDs and CMOS imagers, optical on chip communication, display technologies, TFTs, organic electronics, flexible substrate electronics, SoC and SiP packaging, microsystem packaging. Topics of interest in the MEMS area include resonators, switches, and passives for RF applications, integrated sensors, micro-optical devices, micro-fluidic and biomedical devices, micro power generators and energy harvesting devices, with particular emphasis on integrated implementations.

Optoelectronic and photonic devices

Compound semiconductors (GaAs, InP, GaN, SiC, alloys) and optoelectronic devices, including photovoltaic devices.

Emerging non-CMOS devices and technologies

Nanotubes, nanowires and nanoparticles for electronic, optoelectronic and sensor applications, materials and device related issues, single-electron, molecular and quantum devices, nanophotonics, spintronics, self-assembling methods, photonic devices. New device characterization techniques and performance evaluation methodologies. Energy harvesting.

Carbon-based devices

The latest devices based on carbon carbon nanotubes and graphene. Digital and and analog devices, high frequency devices based on carbon nanotubes and graphene including THz and optoelectronic devices.

PLENARY TALKS

"Automotive electronics and energy efficiency"
Reinhard Ploss, CEO Infineon

"FinFETs: Technology and Circuit Design Challenges"
Min-Reng Lin, Global Foundries

"Carbon electronics for 2020"
Wilfried Haensch, IBM

"Nanometer-scale InGaAs Field-Effect Transistors for THz and CMOS technologies"
J. del Alamo, MIT

"MEMS for automotive and consumer electronics"
Stefan Finkbeiner, Bosch

"Cyborg insects and other things: building interfaces between the synthetic and the multicellular"
M. Maharbiz, UC Berkeley

TUTORIALS AND WORKSHOPS

A tutorial Day will be organized on Monday, 16 September 2013 and a Workshop Day will take place on Friday, 20 September 2013

BEST PAPER AWARDS

Papers presented at the conference will be considered for the Best Paper Award and for the Best "Young Scientist" Paper Award. The selection will be based on the results of the paper selection process and the judgment of the conference participants. The award delivery will take place at ESSDERC 2014.

PAPER SUBMISSION

The 2013 ESSDERC conference will allow only electronic submission of papers in PDF format. Prospective authors must submit their paper(s) via the conference website. Papers must be submitted in the final format to be published in the proceedings. They must not exceed four A4 pages with all illustrations and references included. The size of the PDF files submitted must not exceed 2MB. Manuscript guidelines as well as instructions on how to submit electronically will be available on the conference website.

All paper submissions must be received by 15 April 2013.

After selection of papers, the authors will be informed about the decision of the Technical Program Committee by e-mail by the beginning of June 2013. At the same time, the complete program will be published on the conference website.

The working language of the conference is English, which must also be used for all presentations and printed materials.

Fringe Poster submissions close on 22 June 2013.

REVIEW PROCESS

Papers submitted for review must clearly state:

- The purpose of the work
- How and to what extent it advances the state-of-the-art
- Specific results and their impact

The degree to which the paper deals with the above issues is fundamental to a successful review and selection of the paper. The most frequent cause of rejections is a lack of new results. Only work that has not been previously published will be considered. Submission of a paper for review and subsequent acceptance is considered by the committee as a commitment that the work will not be placed in the public domain prior to the conference.

ESSCIRC / ESSDERC STEERING COMMITTEE

Sorin Cristoloveanu (Chair)	ENSERG-IMEP
Ralf Brederlow (Vice-Chair)	Texas Instruments
Cor Claeys (Executive secretary)	IMEC
Roberto Bez	Micron
Klaas Bult	Broadcom Corporation
Franz Dielacher	Infineon
Athanasios Dimoulas	NCSR Demokritos
Christian Enz	CSEM
Stephen Hall	University of Liverpool
Kazunari Ishimaru	Toshiba America Elect. Comp.
Carlos Mazure	SOITEC
Gaudenzio Meneghesso	University of Padova
Doris Schmitt-Landsiedel	Technical University Munich
Thomas Skotnicki	STMicroelectronics
Hannu Tenhunen	KTH Stockholm
Roland Thewes	TU Berlin